SMART MISSION LAB
by KP Labs

What is Smart Mission Lab?

Smart Mission Lab (SML) is a platform providing remote access to KP Labs' high-performance Data Processing Units, allowing engineers, researchers and developers to **implement and validate AI models, onboard software, and data processing algorithms** without purchasing unknown hardware or setting up complex testing environment.

SML offers a **cost-effective solution** to accelerate mission development. Users can **test KP Labs' DPUs before purchasing,** ensuring compatibility with specific algorithms and mission requirements. By experimenting with different configurations and analyzing real-time performance, engineers can make **informed hardware decisions** while **reducing development time, costs, and risks.**

Discover our platform:

How it makes your life easier?

Traditional Approach	Smart Mission Lab (SML)
Takes several months	Remotely access DPUs within 48 hours
Requires significant one-time investments	Pay-as-you-go with no big investment
Iterations can take weeks or months	Optimize and test edge processing solution within hours
Limited to specific internal setups	Supports FPGA solutions, Linux apps, and ML algorithms
Compatibility issues discovered too late	Validate before purchase, reducing risks
Unclear efficiency of specific edge processing solution	Clear understanding of edge processing outcome

How does it works?

Choose

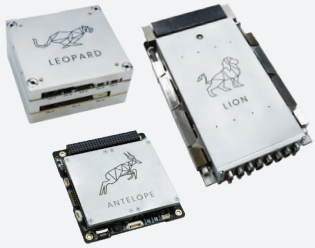
Run your experiment on a real DPU located in our server room

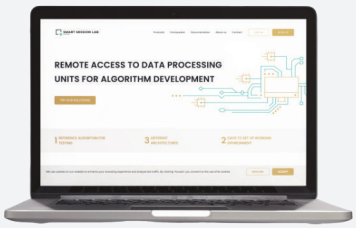
Book

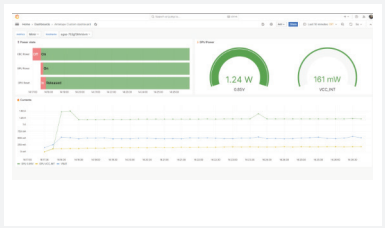
Reserve a DPU via our secure online platform

Test

Deploy, monitor, and optimize your model on real hardware







Compare our DPU's

	Antelope	Leopard	Lion
Size	13.24 x 95.9 x 90.1 mm	95.89 x 90.17 x 47.2 mm	160 mm x 100 mm x 50 mm
Form Factor	PC-104	PC-104	SpaceVPX 3U (mass up to 2.5 kg)
Mass	Around 130-150g	725 g	Around 2.5 kg
Processing Cores	Zynq UltraScale+ MPSoC ZU3/4/5CG: · Dual ARM Cortex-A53 CPU up to 1.5 GHz · Dual ARM Cortex-R5 in lock-step	AMD Zynq UltraScale+ MPSoC ZU6EG | ZU9EG | ZU15EG · Quad ARM Cortex-A53 CPU 1.2 GHz · Dual ARM Cortex-R5 (lock-step) · FPGA for custom function implementation	Xilinx Kintex Ultrascale FPGA KU040
Interfaces	CAN, I2C, GPIO, SPI, RS422/485, UART, LVDS, GTY and GTH transceivers	· Supervisor TMTC interface: CAN with CSP, UART/RS422/485 · PL-connected LVDS, GPIOs and QuadGTH transceivers	CAN, LVDS, SPI, RS422/485, UART, GTY and GTH transceivers
Memory	8-32 GiB DDR4 with ECC	· 16 GiB PS-DDR4 (with ECC) · 64 MB Boot flash (NOR) with TMR · 4 GiB SLC NAND flash memory (with EDAC) · 2 x 320 XSSSB pSLC flash-based mass data storage (redundant)	· 2-8 GiB DDR4 with ECC · 4-32 GiB SLC flash-based file system storage (EDAC) · Up to 4x256 GiB of SLC flash-based data storage

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