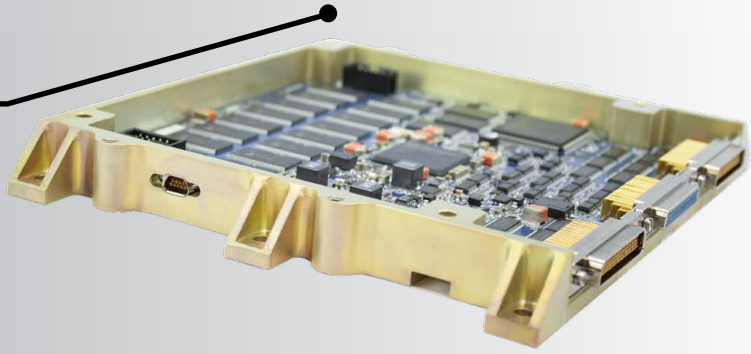
CAVU
AEROSPACE UK

Spacecraft Onboard Computers

OBCM

Satellite On-Board Computer Module



PIONEERING SPACECRAFT COMPUTING

The CAVU OBCM is a state-of-the-art, FPGA-based computing system designed for reliability and efficiency in critical space missions. It offers smooth operation, scalability, and redundancy.

This system is built to withstand various space environments and ensures precise timing, high throughput, and low power consumption for satellite payloads. It also features automatic system recovery and self-diagnosis to keep deep-space missions on track.

KEY FEATURES

- Single Board Flash Based FPGA
- Up to 3 Selectable Boot Regions from Bootloader
- Fully Customizable

INTELLIGENT REDUNDANCY

The OBC is exposed to various hazards in space, such as radiation, cosmic rays, and solar flares, which can cause errors or failures.
CAVU OBCM is designed based on state of the art flash based Microchip/Microsemi SmartFusion2 & ProASIC3 Flash Based FPGA which, according to the company, is SEU immune due to its flash cells architecture.
This architecture also needs less power in comparison with conventional SRAM based FPGA architectures.

ADVANCED SATELLITE COMMAND CONTROL

The OBCM is a highly advanced module designed to meet the complex needs of the satellite industry.
It works with a variety of sensors and actuators for precision control of satellite systems. It supports over 15 different serial interfaces and 200 GPIOs, making it a comprehensive solution for AOCS and Power Management computing needs.
The OBCM offers high levels of control and flexibility, allowing customization to unique requirements. It represents the peak of modern technology in the satellite industry.

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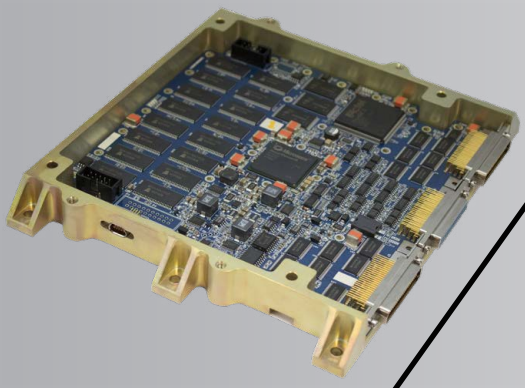

SPECIFICATIONS

SPECIAL FEATURES

Expected Life-time:
3-5 years in LEO
On-Board Current & Temperature Monitoring
On-Board Watchdog
Triple Real Time Clock
Hot Redundant On-Board Voltage Converters
Scalable for Dual Redundancy with Same Module

PROCESSOR

ARM Cortex-M3 on FPGA
Microchip/Microsemi SmartFuion2 Flash Based FPGA
Microsemi ProASIC3 Flash Based FPGA for Interaface
FPU on FPGA Upon Request
150 DMIPS @ 128MHz
SoftConsole/Keil Programming and Debug via JTAG

MEMORY

RAM:
160Mbits MRAM 40 bits width (128Mbits+32Mbits ECC)
ROM:
96Mbits MRAM (Configurable as Triple 32Mbits)
Nonvolatile Flash Memory:
Total 24Gbit SLC NAND Flash (Triple 8G)
256K Serial FRAM
256M Serial NOR

INTERFACES

DIGITAL/ANALOG

Digital Outputs (5V/3.3V)	100
Digital Inputs (5V/3.3V)	90
PWM/Pulse Outputs (5V/3.3V)	10

SERIAL

CAN2.0 Up to 1Mbps	5
Full-Duplex RS422	8
Half-Duplex RS485	8
RS232	1
I2C	1
SPI	1

ENVIRONMENT

Radiation Hardness:
Total Ionizing Dose: 30Krad (Si)/yr
Latch-up Immune
SEE @ 60MeV
Temperature & Pressure:
-40℃ to +85℃ @ 10^{-8} bar
Shocks:
2000g, 2000-10000Hz
Random Vibrations:
14g(RMS) 3-Axis , 20~2000Hz

BUDGET

Dimensions:
203x175x22mm
Mass:
1000gr
Power Supply:
5V ±5%
Power Consumption:
1.5W ~ 3W

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